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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/036,396 | 01/07/2002 | Mutsumi Kimura | 111629 | 3624 |

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| EXAMINER | |
|---|---|
| OSORIO, RICARDO | |
| **ART UNIT** | **PAPER NUMBER** |
| 2673 | |

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/036,396 | KIMURA, MUTSUMI | |
| | Examiner | Art Unit | |
| | RICARDO L OSORIO | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20,23 and 24* is/are pending in the application.

4a) Of the above claim(s) *5,6,14 and 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-13,16-20,23 and 24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07162004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 1, 2, 10, 11, 17, 19, 20, 23 and 24** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huston et al (US 2002/0101396) in view of Tsuboyama et al (5,808,594) and further in view of Yamazaki et al (6,765,549).

**Regarding claims 1, 10, 17, 19, 20**, and **23** Huston teaches of an electro-optical, or display, device to be used in an electronic apparatus comprising a plurality of signal lines; a plurality of scanning lines; pixels disposed in a matrix at intersections of the plurality of signal lines and the plurality of scanning lines (see page 1, paragraph 3, page. 11, paragraph 151, lines 1-8); each of said pixels including a plurality of sub-pixels that are each provided with a static random access memory and an electro-optical element (see page 7, paragraphs 99 and 105, and page 13, paragraph 180, lines 1-7).

However, the device of Huston fails to teach of a size of each of at least two of said sub-pixels being differentiated from each other.

Tsuboyama teaches of a size, or area, of each of at least two sub-pixels, in each pixel, being differentiated from each other (see Figs. 1B, 1C, 8A and 8C, col. 2, lines 16-28 and 53-56, col. 4, lines 23-25, and col. 9, lines 21-32).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have sub-pixels with sizes differentiated from each other, as taught by Tsuboyama, in the device of Huston to obviate an image quality deterioration of so called "false contour" due to an increased number of scanning lines, thereby allowing a high-quality image display (see col. 2, lines 53-56).

Next, the device of Huston teaches of active matrix display including a switching transistor inside a pixel as allowing for higher performance as compared to the passive matrix display (see page 1, paragraph 6).

However, the device of Huston, as anticipated by Tsuboyama, does not precisely teach of a data signal being supplied to the static random access memory through the switching transistor. Yamazaki teaches of a source, or data signal, (Fig. 3, reference character 107) as being supplied to an SRAM (Fig. 3, reference character 108) through a switching transistor having a gate connected to a scanning line (Fig. 3, reference character 105) inside the pixel (Fig. 3, reference character 104).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to supply the data signal to the SRAM through a switching transistor, as taught by Yamazaki, in the combined device of Huston and Tsuboyama because switching transistors integrated into the pixel circuits, or sub-pixels, are widely known as active matrix displays, in the art of display devices, and are widely known to greatly improve the performance of the display by improving the response speed, angle of visibility and contrast, and reducing power consumption, among other benefits.

**Regarding claims 2 and 11**, furthermore, Huston teaches of said sub-pixels, or electro-optical elements, receiving data supplied to control a luminance level being set in one of an On, higher luminance level, or state, and an OFF, lower luminance level, or state (page 7, paragraph 105. Although not specifically mentioned, it is inherent that the sub-pixel will at least be On or OFF).

**Regarding claim 24**, further, the device of Huston, as anticipated by Tsuboyama, does not precisely teach of an electro-optical element disposed between the switching transistor and the static random access memory.

Yamazaki teaches, (in Fig. 18, reference characters 1701, 1704 and 1703, and in col. 2, lines 8-16) an electro-optical element disposed between a switching transistor and a memory.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the electro-optical element disposed between the transistor and the memory, as taught by Yamazaki, in the combined device of Huston and Tsuboyama because this pixel structure of an active matrix EL display is conventionally known in the art (see Yamazaki, col. 2, lines 8-16).

3. **Claims 3-4 and 12-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huston in view of Tsuboyama and Yamazaki as applied to claims 1, 2, 10, 11, 17, 19 and 20 above, and further in view of Sato et al (5,357,583).

**Regarding claims 3 and 12**, further, the device of Huston, as anticipated by Tsuboyama and Yamazaki, does not precisely teach of a greyscale level being set by a function of a ratio of a maximum luminance level of each of the pixels to a sum of luminance levels of all the sub-pixels, or electro-optical elements, included, or contained, in each of the pixels.

Sato teaches of a greyscale level being set by a function of a ratio of a maximum luminance level of each of the pixels to a sum of luminance levels of all the sub-pixels, or electro-optical elements, included, or contained, in each of the pixels (col. 5, lines 55-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the luminance ratio and the sum of luminance levels, as taught by Sato, in the combined device of Huston, Tsuboyama and Yamazaki because this luminance ratio and sum of luminance levels method is a well known in the art of ratio gradation methods (col. 5, line 52).

**Regarding claims 4 and 13**, further, the device of Huston as anticipated by Tsuboyama and Yamazaki, does not precisely teach of a grayscale level being set by a function of a ratio of an area occupied by each of said pixels, or by all the electro-optical elements contained in one of said pixels, to a total area occupied by the sub-pixels in the ON state included in the each of said pixels, or by the electro-optical elements set at the higher luminance level.

Sato teaches of a grayscale level being set by a function of a ratio of an area occupied by each of said pixels, or by all the electro-optical elements contained in one of said pixels, to a total area occupied by the sub-pixels in the ON state included in the each of said pixels, or by the electro-optical elements set at the higher luminance level (col. 5, lines 55-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the area ratio, as taught by Sato, in the combined device of Huston, Tsuboyama and Yamazaki because this area ratio method is a well known in the art of ratio gradation methods (col. 5, line 52).

4. **Claims 7 and 16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huston in view of Tsuboyama and Yamazaki as applied to claims 1, 2, 10, 11, 17, 19 and 20 above, and further in view of Alt et al (6,697,037).

**Regarding claims 7 and 16**, Huston teaches that said electro-optical elements can include LCDs, spatial light modulators, gratings, mirror light valves, and LED arrays (page 6, paragraph 90).

However, the device of Huston, as anticipated by Tsuboyama and Yamazaki, does not specifically include electroluminescent arrays.

Alt teaches of electro-optical elements including subpixel SRAM memories for electroluminescent arrays (col. 6, lines 37-48 and col. 9, lines 1-5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the electroluminescent elements, as taught by Alt, in the combined device of Huston, Tsuboyama and Yamazaki because EL elements are just another example of pixel element arrays with the SRAM memories.

5. **Claims 8-9 and 18** are rejected under 35 U.S.C. 103(a) as being unpatentable over Huston in view of Tsuboyama and Yamazaki and further in view of Sato et al (5,357,583).

**Regarding claims 9, and 18** (see rejection of claims 1, 10 and 17 in paragraph 4 above), further, Huston, as anticipated by Tsuboyama and Yamazaki, does not precisely teach of obtaining a greyscale by using a ratio of a maximum luminance level of each of said pixels to a sum of luminance levels of the sub-pixels in the ON state included in each of said pixels.

Sato teaches of obtaining a greyscale by using a ratio of a maximum luminance level of each of said pixels to a sum of luminance levels of the sub-pixels in the ON state included in each of said pixels (col. 5, lines 55-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the luminance ratio, as taught by Sato, in the combined device of Huston, Tsuboyama and Yamazaki because this luminance ratio method is a well known in the art ratio gradation methods (col. 5, line 52).

**Regarding claim 8**, (see rejection of claims 1, 10 and 17 in paragraph 4 above), further, Huston, as anticipated by Tsuboyama and Yamazaki, does not precisely teach of obtaining a grayscale by using a ratio of an area occupied by each of said pixels to a total area occupied by the sub-pixels in the ON state included in each of said sub-pixels.

Sato teaches of obtaining a grayscale by using a ratio of an area occupied by each of said pixels to a total area occupied by the sub-pixels in the ON state in each of said sub-pixels (col. 5, lines 55-59).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the area ratio, as taught by Sato, in the device of Huston, Tsuboyama and Yamazaki because this area ratio method is a well known in the art ratio gradation method (col. 5, line 52).

### *Response to Arguments*

6. Applicant's arguments with respect to claims 1, 8-10, 17 and 18 have been considered but are moot in view of the new ground(s) of rejection (see above rejection).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ricardo L. Osorio whose telephone number is 703 305-2248. The examiner can normally be reached on Monday through Thursday from 7:00 A.M. to 5:30 P.M. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala whose telephone number is 703 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to: 703 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ricardo L. Osorio
Examiner
Art Unit: 2673

RLO
April 16, 2005